IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application : **09/936,185**

Applicant(s) : **KELLY et al.**

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Examiner : **VENT, Jamie J.**

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Title: **METHOD OF SETTING A SYSTEM TIME CLOCK AT THE START OF AN MPEG SEQUENCE**

Mail Stop: **APPEAL BRIEF - PATENTS**
Commissioner for Patents
Alexandria, VA 22313-1450

APPEAL UNDER 37 CFR 41.37

Sir:

This is an appeal from the decision of the Examiner dated 1 November 2001, finally rejecting claims 1-5 and 7-21 of the subject application.

This paper includes (each beginning on a separate sheet):

1. **Appeal Brief;**
2. **Claims Appendix;**
3. **Evidence Appendix; and**
4. **Related Proceedings Appendix.**

APPEAL BRIEF

I. REAL PARTY IN INTEREST

The above-identified application is assigned, in its entirety, to **Koninklijke Philips Electronics N. V.**

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any co-pending appeal or interference that will directly affect, or be directly affected by, or have any bearing on, the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claim 6 is canceled.

Claims 1-5 and 7-21 are pending in the application.

Claims 1-5 and 7-21 stand rejected by the Examiner under 35 U.S.C. 103(a).

These rejected claims are the subject of this appeal.

IV. STATUS OF AMENDMENTS

An amendment was filed on 14 March 2007, subsequent to the final rejection in the Office Action dated 1 November 2007, canceling claim 6.

V. SUMMARY OF CLAIMED SUBJECT MATTER

This invention addresses the processing of time-based information, such as an MPEG audio/video transport stream. In an example embodiment, the method and system of this invention provide means for processing the time-based information in the absence of a clock reference, such as when a stream is first being received, or when different streams are being merged during editing to create new streams (Applicants' specification, page 1, 9-20; FIGs. 1 and 2). MPEG transport streams periodically include a Program Clock Reference (PCR) in select packets for locking a local system clock; however, in the case of initially receiving packets from a continuous stream, packets that arrive before a first Program Clock Reference is received are not yet synchronized to the local system clock, and the time at which they should be rendered is unknown (page 1, lines 10-12). In an embodiment of this invention, means are provided for determining the proper system clock time corresponding to the start of reception of the stream, thereby allowing the initial packets to be subsequently rendered at the proper time sequence (page 1, lines 28-29). A time stamp having an arbitrary starting value is appended to each received packet, and the value of the time stamp appended to the first packet that includes a Program Clock Reference (to which the system clock is subsequently locked) is used to establish a correspondence between each packet and the system clock, including the packets received prior to receipt of the Program Clock Reference (page 3, lines 24-32). The determined value of the system clock at the start of the stream, relative to the Program Clock Reference, is termed the System Time Counter Start time, STC-start. If the stream is stored for subsequent rendering, the STC-start time is also stored, preferably as a segment attribute, to facilitate rapid synchronization for playback (page 3, lines 32-33; page 4, lines 19-22). In the case of a discontinuity caused by merging streams with different clock references, similar techniques are used, albeit using multiple STC-start time determinations (page 4, line 28 – page 5, line 14).

As claimed in independent claim 1, an embodiment of the invention comprises a method comprising:

determining a packet arrival time of each packet of a received sequence of information signal packets (TS packet) comprising A/V information using a packet arrival time counter derived from a local System Time Counter (STC), the received sequence including, at intervals of multiple information signal packets, Program Clock Reference (PCR) information that facilitates locking the local System Time Counter (STC) with the Program Clock Reference (PCR) information (page 3, lines 13-23; FIG. 3),

appending a Packet Arrival Timestamp (PAT) corresponding to the packet arrival time to each packet (page 3, lines 24-25),

setting the packet arrival time counter at an initial value before receiving a first information signal packet (page 3, line 24),

determining a first Packet Arrival Timestamp (PAT) of the first information signal packet of the sequence and a second Packet Arrival Timestamp (PAT) of a first information signal packet that includes a Program Clock Reference (PCR) value (page 3, lines 26-28),

determining a number of counts of the local System Time Clock Counter (STC) between the first and the second Packet Arrival Timestamps (PAT) (page 3, lines 28-29), and

determining a System Time Counter start value (STC-start) by subtracting the number of counts from the Program Clock Reference (PCR) value (page 3, lines 29-31).

As claimed in dependent claim 2, an embodiment of the invention comprises the method of claim 1, including

storing the received information signal packets with the appended Packet Arrival Time Stamps (PAT) on a recording medium (page 3, line 33), and

storing the System Time Counter start value (STC-start) as an attribute of the stored received information signal packets with the appended Packet Arrival Time Stamps (PAT) (page 3, line 31-33).

As claimed in independent claim 3, an embodiment of the invention comprises a method comprising (FIGs. 5 and 8):

running a packet arrival time counter (20) derived from a local System Time Counter (STC) (17) (page 3, lines 22-23),

locking the local System Time Counter (STC) to retrieved Program Clock Reference (PCR) information (page 3, lines 16-18),

retrieving information signal packets and their corresponding Packet Arrival Timestamps (PAT) from a storage medium (page 6, lines 1-5; page 4, lines 1-3),

storing a number of retrieved information signal packets (page 4, lines 7-8; 47 in FIG. 8),

outputting an information signal packet when the corresponding Packet Arrival Timestamp (PAT) coincides with the packet arrival time counter (page 6, lines 10-14),

retrieving a System Time Counter start value (STC-start) from the storage medium (page 4, lines 19-21; page 6, lines 8-10), and

setting the System Time Counter (STC) with the retrieved System Time Counter start value (STC-start) (page 4, lines 19-21; page 6, lines 8-10).

As claimed in independent claim 5, an embodiment of the invention comprises a method comprising: (FIGs. 6 and 8)

running a presentation time counter derived from a local System Time Counter (STC) (FIGs. 3 and 5; page 5, lines 13-17; page 3, lines 22-23),

locking the local System Time Counter (STC) to retrieved Program Clock Reference (PCR) information corresponding to either a first sequence or a second sequence of information signal packets (TS) comprising A/V information (page 4, lines 19-22),

retrieving information signal packets and their corresponding Presentation Time Stamps (PTS) from a storage medium (page 6, 3-5),

storing a number of retrieved signal information packets (page 4, lines 7-8; 47 in FIG. 8),

presenting an information signal packet when the corresponding Presentation Time Stamp (PTS) coincides with the presentation time counter (page 6, lines 10-14),

subtracting a System Time Counter start value (STC-start-2) of the second sequence from a value of the Presentation Time Stamp (PTS) of a first information signal packet of the second sequence (page 5, lines 11-13), and

setting the local System Time Counter (STC) to the value of the System Time Counter start value (STC-start-2) (page 5, lines 13-14).

As claimed in independent claim 9, an embodiment of the invention comprises a method of storing a real time sequence of information signal packets comprising A/V information, on a record carrier, the sequence comprising Program Clock Reference (PCR) information for locking a local System Time Counter (STC), Presentation Time Stamp (PTS) information for determining the presentation time of the information comprised in the information signal packets, Decoding Time Stamp (DTS) information for determining the decoding time of the information comprised in the information signal packets, and Packet Identification (PID) mapping information, the method comprising:

adding mark points at specific entry points in the sequence (page 6, lines 17-19), and

storing the mark point and one or more of the following information entities: Program Clock Reference (PCR) information, Presentation Time Stamp (PTS) information, Decoding Time Stamp (DTS) information, and Packet Identification (PID) mapping information (page 6, line 32 – page 7, line 1).

As claimed in independent claim 13, an embodiment of the invention comprises a system comprising: (FIG. 7)

a receiver (35) that is configured to receive a sequence of information signal packets, the received sequence including, at intervals of multiple signal packets, program clock reference information (page 5, lines 17-20),

a timestamp generator (15) that is configured to provide a packet arrival timestamp corresponding to each information signal packet (page 5, lines 20-22; page 3, lines 24-26),

a combiner (38) that is configured to append the packet arrival timestamp to each corresponding information signal packet (page 5, lines 23-25), and

a packet detector (36) that is configured to detect a program clock reference value in a clock referencing information signal packet that includes program clock reference information (page 5, lines 18-20),

wherein

the timestamp generator (15) is configured to provide a system time start value based on the program clock reference value and a time difference between the clock referencing information signal packet and an initial information signal packet (page 5, lines 20-22; page 3, lines 29-33), and

the combiner (38) is configured to associate the system start time with the sequence of information packets (page 5, lines 23-25).

As claimed in dependent claim 14, an embodiment of the invention comprises the system of claim 13, including a writer (41) that is configured to write the sequence of information packets with appended packet arrival timestamps and associated system start time to a recording medium (page 5, lines 25-27).

As claimed in independent claim 17, an embodiment of the invention comprises a system comprising: (FIG. 8)

a reader (44) that is configured to read a sequence of information packets and an associated system start time, each packet of the sequence of information packets including a corresponding packet arrival timestamp, and select packets including a program clock reference value (page 6, lines 3-5; page 3, lines 3-5),

a buffer (47) that is configured to store the sequence of information packets (page 4, lines 7-8; page 6, line 12), and

a controller (38) that is configured to control an output of the buffer to provide the sequence of information packets in a time sequence that is dependent upon the system start time and the packet arrival timestamps (page 6, lines 8-14).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-5 and 7-21 stand rejected under 35 U.S.C. 103(a) over Dieterich et al. (USP 6,208,643, hereinafter Dieterich), Miyazawa (USP 6,542,518), and Fujii et al. (USP 5,898,695, hereinafter Fujii).

VII. ARGUMENT

Claims 1-5 and 7-21 stand rejected under 35 U.S.C. 103(a) over Dieterich, Miyazawa, and Fujii

MPEP 2142 states:

> "To establish a *prima facie* case of obviousness … the prior art reference (or references when combined) ***must teach or suggest all the claim limitations***… If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness."

Claims 1-2, 7, and 11

The combination of Dieterich, Miyazawa, and Fujii fails to teach or suggest determining a first Packet Arrival Timestamp (PAT) of a first information signal packet of a sequence and a second Packet Arrival Timestamp (PAT) of a first information signal packet that includes a Program Clock Reference (PCR) value, fails to teach or suggest determining a number of counts of the local System Time Clock Counter (STC) between the first and the second Packet Arrival Timestamps (PAT), and fails to teach or suggest determining a System Time Counter start value (STC-start) by subtracting the number of counts from the Program Clock Reference (PCR) value, as specifically claimed in claim 1, upon which claims 2, 7, and 11 depend.

The Office action asserts that Dieterich teaches "determining a System Time Counter start value (STC-start) by subtracting the number of counts of the local System Time Counter (STC) subtracting this number from the Program Clock Reference (PCR) value to retrieve a System Time Counter start value (STC-start)" [sic] (Office action, page 3, lines 12-15). The applicants respectfully disagree with this assertion.

The Office action notes that at column 2, lines 30+, Dieterich "describes the determination of number of counts of the STC through the subtraction of variables". However, the applicants respectfully maintain that the act of subtracting variables does not support the Office action's assertion that Dieterich teaches the determination of an STC-start value as claimed. Of particular note, Dieterich's equation at column 2, line 52 determines the system time counter corresponding to

the receipt of a PCR, based on the time of receipt of a prior PCR and a frequency correction factor.

Of particular note, Dieterich specifically teaches that "the present invention tracks only the time of reception of the PCR and packets of that particular PID" (Dieterich, column 2, lines 29-31). At FIG. 3, Dieterich's timing analysis (325, 330) starts only after receipt of a packet that contains a PCR (315; column 6, lines 8-18). Dieterich does not teach or suggest determining a start time of a first packet that arrives before a first packet that contains a PCR arrives, and does not teach subtracting values to obtain such a start time, as specifically claimed in claim 1.

The Office action acknowledges that Dieterich fails to teach appending a Packet Arrival Timestamp (PAT) corresponding to a packet arrival time of each packet, fails to teach determining a first Packet Arrival Timestamp (PAT) of a first information signal packet of the sequence, and fails to teach determining a first Packet Arrival Timestamp (PAT) of a first information signal packet containing Program Clock Reference (PCR) information, and relies on Miyazawa for this teaching.

The Office action asserts that Miyazawa "discloses a system wherein the information corresponding to the PAT is received, stored, and used in determining information in regards to the timestamp" (Office action, page 4, lines 1-2). The applicants respectfully disagree with this assertion.

In the applicants' claims, the term PAT corresponds to a "Packet Arrival Timestamp". In Miyazawa, the term PAT corresponds to a "Program Association Table":

> The PAT (Program Association Table) is information that represents packet identification information PID of the TS packet that has the PMT generated for each program.
> The PAT is composed of a table ID (identifier) (8 bits) (that represents the type of a table defined in MPEG2 standard), a section syntax indicator (1 bit), "0" data (1 bit), a reserved portion (2 bits), a section length (12 bits), a transport stream (TS) ID (16 bits), a reserved portion (2 bits), a version number (5 bits), a current next indicator (1 bit), a section number (8 bits), a last section number (8 bits), a program number (16 bits), a reserved portion (3 bits), a network PID (13 bits) or a program map (PID) (13 bits), and a CRC

> (Cyclic Redundancy Check) (32 bits). Thus, the data size of the PAT is around 16 bytes." (Miyazawa, column 13, lines 44-58.)

As is clearly evident, Miyazawa's Program Association Table does not relate to a timestamp, and does not correspond to the applicants' claimed Packet Arrival Timestamp.

The Office action also asserts that Fujii teaches "the ability to determine the PAT of various information signals as seen in Figure 18" (page 4, liens 5-6). The applicants respectfully disagree with this assertion, and respectfully note that a broad reference to a figure does not comply with the requirements of MPEP 707 (c)(2):

> "When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified."

The pertinence of Fujii's FIG. 18 is not apparent, and the Office action fails to identify the particular parts relied upon, and fails to identify the specific elements of the applicants' claim to which such parts are asserted to correspond.

Because the combination of Dieterich, Miyazawa, and Fujii fails to teach each of the elements of claim 1, upon which claims 2, 7, and 11 depend, the applicants respectfully maintain that the rejection of claims 1-2, 7, and 11 under 35 U.S.C. 103(a) over Dieterich, Miyazawa, and Fujii is unfounded, per MPEP 2142, and should be reversed by the Board.

Claim 2

The combination of Dieterich, Miyazawa, and Fujii fails to teach or suggest storing the received information signal packets with the appended Packet Arrival Time Stamps (PAT) on a recording medium, and storing the System Time Counter start value (STC-start) as an attribute of the stored received information signal packets with the appended Packet Arrival Time Stamps (PAT).

The Office action acknowledges that Dieterich fails to teach storing the Packet Arrival Time Stamps (PAT) on a recording medium, and asserts that Miyazawa provides this teaching. The applicants respectfully disagree with this assertion. As noted above, Miyazawa's Program Association Table does not relate to a timestamp, and does not correspond to the applicants' claimed Packet Arrival Timestamp. Accordingly, the applicants respectfully maintain that the rejection of claim 2 under 35 U.S.C. 103(a) over Dieterich, Miyazawa, and Fujii is unfounded, per MPEP 2142, and should be reversed by the Board.

Claims 3-4, 8, and 12

The Office action fails to identify where the combination of Dieterich, Miyazawa, and Fujii teaches or suggests retrieving information signal packets and their corresponding Packet Arrival Timestamps (PAT) from a storage medium, fails to identify where the combination teaches or suggests retrieving a System Time Counter start value (STC-start) from the storage medium, and fails to identify where the combination teaches or suggests setting the System Time Counter (STC) with the retrieved System Time Counter start value (STC-start), as specifically claimed in claim 3, upon which claims 4, 8, and 12 depend. Accordingly, the applicants respectfully maintain that the rejection of claims 3-4, 8, and 12 under 35 U.S.C. 103(a) over Dieterich, Miyazawa, and Fujii is unfounded, per MPEP 2142, and should be reversed by the Board.

Claims 5 and 21

The Office action fails to identify where the combination of Dieterich, Miyazawa, and Fujii teaches or suggests retrieving information signal packets and their corresponding Presentation Time Stamps (PTS) from a storage medium, fails to identify where the combination of Dieterich, Miyazawa, and Fujii teaches or suggests subtracting a System Time Counter start value (STC-start-2) of a second sequence from a value of the Presentation Time Stamp (PTS) of a first information signal packet of the second sequence, and fails to identify where the combination of

Dieterich, Miyazawa, and Fujii teaches or suggests setting the local System Time Counter (STC) to the value of the System Time Counter start value (STC-start-2), as specifically claimed in claim 5, upon which claim 21 depends. Accordingly, the applicants respectfully maintain that the rejection of claims 5 and 21 under 35 U.S.C. 103(a) over Dieterich, Miyazawa, and Fujii is unfounded, per MPEP 2142, and should be reversed by the Board.

Claims 9-10

The combination of Dieterich, Miyazawa, and Fujii fails to teach or suggest adding mark points at specific entry points in the sequence, and storing the mark point and one or more of the following information entities: Program Clock Reference (PCR) information, Presentation Time Stamp (PTS) information, Decoding Time Stamp (DTS) information, and Packet Identification (PID) mapping information, as specifically claimed in claim 9, upon which claim 10 depends.

The Office action asserts that Dieterich provides this teaching at FIG. 10 and column 15 line 53 through column 16 line 37, but provides no basis for this assertion. Dieterich's FIG. 10 and the accompanying text address the processing of Service Information (SI) tables, and do not address adding mark points and other information entities at specific entry points in a sequence, as specifically claimed in claim 9. Accordingly, the applicants respectfully maintain that the rejection of claims 9 and 10 under 35 U.S.C. 103(a) over Dieterich, Miyazawa, and Fujii is unfounded, per MPEP 2142, and should be reversed by the Board.

Claims 13-16

The combination of Dieterich, Miyazawa, and Fujii fails to teach or suggest a combiner that is configured to append a packet arrival timestamp to each corresponding information signal packet, and fails to teach or suggest a timestamp generator that provides a system time start value based on the program clock reference value and a time difference between the clock referencing information signal packet and an initial information signal packet, and fails to teach or suggest

that the combiner is configured to associate the system start time with the sequence of information packets, as specifically claimed in claim 13, upon which claims 14-16 depend.

The Office action asserts that Dieterich's microprocessor 240 appends a packet arrival timestamp to each corresponding information signal packet, but provides no basis for this assertion.

The Office action asserts that Dieterich's timestamp generator 230 provides a system time start value based on the program clock reference value and a time difference between the clock referencing information signal packet and an initial information signal packet, but provides no basis for this assertion, other than "Column 4, lines 53+ describes the timestamp generator".

The Office action fails to identify where the combination of Dieterich, Miyazawa, and Fujii teaches or suggests that the combiner is configured to associate the system start time with the sequence of information packets.

Because the Office action fails to specifically identify where the combination of Dieterich, Miyazawa, and Fujii teaches or suggests each of the elements of claim 13, the applicants respectfully maintain that the rejection of claims 13-16 under 35 U.S.C. 103(a) over Dieterich, Miyazawa, and Fujii is unfounded, per MPEP 2142, and should be reversed by the Board.

Claims 14-15

The combination of Dieterich, Miyazawa, and Fujii fails to teach or suggest a writer that is configured to write a sequence of information packets with appended packet arrival timestamps and associated system start time to a recording medium, as claimed in claim 14, upon which claim 15 depends.

The Office action asserts that Dieterich provides this teaching at column 4, lines 32-40. At the cited text, Dieterich teaches:

> "Returning to FIG. 2, the bitstream analyzer 200 comprises an input buffer 210, a buffer controller 220, a counter 230, a processor 240, a memory 250 and a display 260. More specifically, the bitstream analyzer receives as an input a real-time digital bitstream on path 205, such as an MPEG transport stream, carrying clock information in the form of PCR data and an indicator of

> the "start of packet", e.g., MPEG provides that the first byte of each packet shall be a value of "47" (hex). This predefined value allows the decoder to detect the start of a packet."

As can be seen, the cited text fails to address a packet arrival timestamp, and cannot be said to teach or suggest writing a sequence of information packets with appended packet arrival timestamps and associated system start time to a recording medium, as claimed in claim 14. Accordingly, the applicants respectfully maintain that the rejection of claims 14-15 under 35 U.S.C. 103(a) over Dieterich, Miyazawa, and Fujii is unfounded, per MPEP 2142, and should be reversed by the Board.

Claims 17-20

The combination of Dieterich, Miyazawa, and Fujii fails to teach or suggest a reader that is configured to read a sequence of information packets and an associated system start time, each packet of the sequence of information packets including a corresponding packet arrival timestamp, and fails to teach or suggest a controller that is configured to control an output of a buffer to provide the sequence of information packets in a time sequence that is dependent upon the system start time and the packet arrival timestamps, as claimed in claim 17, upon which claims 18-20 depend.

The Office action asserts that Dieterich provides these teachings at column 4, line 32 – column 5, line 16, but provides no basis for these assertions other than to state that "Column 4, lines 32+ describes the hardware involved in the reading of information packets", "Lines 48+ describes the FIFO for storing the information packets", and "Lines 52+ and Column 5 Lines 1-16 describes the comparison of timestamps". These broad assertions do not comply with the requirement of MPEP 707 (c)(2) to specifically and particularly identify where each element is found in the prior art. Accordingly, the applicants respectfully maintain that the rejection of claims 14-15 under 35 U.S.C. 103(a) over Dieterich, Miyazawa, and Fujii is unfounded, per MPEP 2142, and should be reversed by the Board.

CONCLUSIONS

Because the Office action fails to identify where each element of each of the applicants' claims is taught or suggested in the combination of Dieterich, Miyazawa, and Fujii, the applicants respectfully request that the Examiner's rejection of claims 1-5 and 7-21 under 35 U.S.C. 103(a) over Dieterich, Miyazawa, and Fujii be reversed by the Board, and the claims be allowed to pass to issue.

Respectfully submitted

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CLAIMS APPENDIX

1. A method comprising:

determining a packet arrival time of each packet of a received sequence of information signal packets (TS packet) comprising A/V information using a packet arrival time counter derived from a local System Time Counter (STC), the received sequence including, at intervals of multiple information signal packets, Program Clock Reference (PCR) information that facilitates locking the local System Time Counter (STC) with the Program Clock Reference (PCR) information,

appending a Packet Arrival Timestamp (PAT) corresponding to the packet arrival time to each packet,

setting the packet arrival time counter at an initial value before receiving a first information signal packet,

determining a first Packet Arrival Timestamp (PAT) of the first information signal packet of the sequence and a second Packet Arrival Timestamp (PAT) of a first information signal packet that includes a Program Clock Reference (PCR) value,

determining a number of counts of the local System Time Clock Counter (STC) between the first and the second Packet Arrival Timestamps (PAT), and

determining a System Time Counter start value (STC-start) by subtracting the number of counts from the Program Clock Reference (PCR) value.

2. The method of claim 1, including

storing the received information signal packets with the appended Packet Arrival Time Stamps (PAT) on a recording medium, and

storing the System Time Counter start value (STC-start) as an attribute of the stored received information signal packets with the appended Packet Arrival Time Stamps (PAT).

3. A method comprising

running a packet arrival time counter derived from a local System Time Counter (STC),

locking the local System Time Counter (STC) to retrieved Program Clock Reference (PCR) information,

retrieving information signal packets and their corresponding Packet Arrival Timestamps (PAT) from a storage medium,

storing a number of retrieved information signal packets,

outputting an information signal packet when the corresponding Packet Arrival Timestamp (PAT) coincides with the packet arrival time counter,

retrieving a System Time Counter start value (STC-start) from the storage medium, and

setting the System Time Counter (STC) with the retrieved System Time Counter start value (STC-start).

4. The method of claim 3, including inserting Program Clock Reference (PCR) information corresponding to the System Time Counter start value (STC-start).

5. A method comprising

running a presentation time counter derived from a local System Time Counter (STC),

locking the local System Time Counter (STC) to retrieved Program Clock Reference (PCR) information corresponding to either a first sequence or a second sequence of information signal packets (TS) comprising A/V information,

retrieving information signal packets and their corresponding Presentation Timestamps (PTS) from a storage medium,

storing a number of retrieved signal information packets,

presenting an information signal packet when the corresponding Presentation Timestamp (PTS) coincides with the presentation time counter,

subtracting a System Time Counter start value (STC-start-2) of the second sequence from a value of the Presentation Timestamp (PTS) of a first information signal packet of the second sequence, and

setting the local System Time Counter (STC) to the value of the System Time Counter start value (STC-start-2).

6. (Canceled)

7. Apparatus for recording a real time sequence of information signal packets (TS packet) comprising A/V information, on a record carrier, the serial sequence comprising at intervals of multiple information signal packets, Program Clock Reference (PCR) information for locking a local System Time Counter (STC) with the Program Clock Reference (PCR) information, the apparatus comprising

receiving means for receiving the information signal packets,

time stamp generating means for generating a time stamp corresponding to an arrival time of the information signal packets,

writing means for recording the generated time stamps and information signal packets on the record carrier, the time stamp generating means provided with a system time counter locked to the received program clock reference (PCR) information, wherein

the time stamp generating means are adapted to generate time stamps according to the method of claim 1.

8. Apparatus for reproducing a real time sequence of information signal packets (TS packet) comprising A/V information recorded on a record carrier the apparatus comprising

reading means for reading the information signal packets recorded on the record carrier,

storing means for temporarily storing a number of information signal packets read from the record carrier,

time stamp generation means comprising a Packet Arrival Time counter derived from a local System Time Counter (STC),

comparator means for comparing a stored time stamp of an information signal packet with the generated Packet Arrival Time value,

outputting an information signal packet from the storing means when a Packet Arrival Time Counter value coincides with the corresponding time stamp, characterized in that,

the time stamp generating means are adapted to generate a Packet Arrival Time according to the method of claim 3.

9. Method of storing a real time sequence of information signal packets comprising A/V information, on a record carrier, the sequence comprising Program Clock Reference (PCR) information for locking a local System Time Counter (STC), Presentation Time Stamp (PTS) information for determining the presentation time of the information comprised in the information signal packets, Decoding Time Stamp (DTS) information for determining the decoding time of the information comprised in the information signal packets, and Packet Identification (PID) mapping information, the method comprising:

adding mark points at specific entry points in the sequence,

storing the mark point and one or more of the following information entities: Program Clock Reference (PCR) information, Presentation Time Stamp (PTS) information, Decoding Time Stamp (DTS) information, and Packet Identification (PID) mapping information.

10. The method of claim 9, wherein the entry points include I-frames in an MPEG sequence of encoded frames.

11. The method of claim 1, wherein the received sequence corresponds to a sequence of MPEG encoded frames.

12. The method of claim 3, wherein the received sequence corresponds to a sequence of MPEG encoded frames.

13. A system comprising:

a receiver that is configured to receive a sequence of information signal packets, the received sequence including, at intervals of multiple signal packets, program clock reference information,

a timestamp generator that is configured to provide a packet arrival timestamp corresponding to each information signal packet,

a combiner that is configured to append the packet arrival timestamp to each corresponding information signal packet, and

a packet detector that is configured to detect a program clock reference value in a clock referencing information signal packet that includes program clock reference information,

wherein

the timestamp generator is configured to provide a system time start value based on the program clock reference value and a time difference between the clock referencing information signal packet and an initial information signal packet, and

the combiner is configured to associate the system start time with the sequence of information packets.

14. The system of claim 13, including a writer that is configured to write the sequence of information packets with appended packet arrival timestamps and associated system start time to a recording medium.

15. The system of claim 14, wherein the sequence of information packets correspond to a sequence of MPEG-encoded packets, and the system start time is recorded as a segment attribute.

16. The system of claim 13, wherein the timestamp generator includes

an oscillator,

a system counter, operably coupled to the oscillator, that is configured to provide a local clock reference,

a phase detector that is configured to control an output of the oscillator based on a comparison of the local clock reference to the program clock reference value, and

a packet timestamp generator, operably coupled to the output of the oscillator, that is configured to provide the packet arrival timestamps.

17. A system comprising:

a reader that is configured to read a sequence of information packets and an associated system start time, each packet of the sequence of information packets including a corresponding packet arrival timestamp, and select packets including a program clock reference value,

a buffer that is configured to store the sequence of information packets, and

a controller that is configured to control an output of the buffer to provide the sequence of information packets in a time sequence that is dependent upon the system start time and the packet arrival timestamps.

18. The system of claim 17, including

a timestamp generator that is configured to provide a local timestamp for each information packet based on the system start time,

wherein,

the controller is configured to provide the output of the buffer based on a comparison of the local timestamp and the packet arrival timestamp of each information packet.

19. The system of claim 18, including a demultiplexer, operably coupled to the controller and the timestamp generator, that is configured to extract the system start time, the program clock reference value, and the packet arrival timestamps from the sequence of information packets.

20. The system of claim 18, wherein the timestamp generator includes

an oscillator,

a system counter, operably coupled to the oscillator, that is configured to provide a local clock reference,

a phase detector that is configured to control an output of the oscillator based on a comparison of the local clock reference to the program clock reference value, and

a packet timestamp generator, operably coupled to the output of the oscillator, that is configured to provide the local timestamps,

wherein

the controller is configured to set the system counter to an initial value corresponding to the system start time.

21. The method of claim 5, wherein the first and second sequences correspond to sequences of MPEG-encoded frames.

EVIDENCE APPENDIX

No evidence has been submitted that is relied upon by the appellant in this appeal.

RELATED PROCEEDINGS APPENDIX

Appellant is not aware of any co-pending appeal or interference which will directly affect or be directly affected by or have any bearing on the Board's decision in the pending appeal.